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APPLICANT Collaert, et al.		
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U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
T.D	1	8,118,161	09/12/00	Chapman, et al.	—	—	/
T.D	2	6,207,511	03/27/01	Chapman, et al.	—	—	
T.D	3	6,252,284 B1	06/26/01	Muller, et al.	—	—	

EXAMINER INITIAL	OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)						
T.D	4	Choi, et al., "Nanoscale CMOS Spacer FinFET for the Terabit Era", IEEE Electron Device Letters, vol. 23, no. 1, pp. 25-27, (January 2002).					
	5	Choi, et al., "Sub-20nm CMOS FinFET Technologies", IEEE, pp. 421-424, (2001).					
	6	Hisamoto, et al., "A Folded-channel MOSFET for Deep-sub-tenth Micron Era", International Electron Devices Meeting, pp. 1032-1034, (1998).					
	7	Huang, et al., "Sub-50 nm P-Channel FinFET", IEEE Transactions on Electron Devices, vol. 48, no. 5, pp. 880-886, (May 2001).					
	8	Kedzierski, et al., "High-performance symmetric-gate and CMOS-compatible V _t asymmetric-gate FinFET devices", IEEE, pp. 437-440, (2001).					
T.D	9	European Search Report dated December 17, 2002 for European Application No. 02 44 7135.1.					

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EXAMINER T. DANG	DATE CONSIDERED 10/12/04
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